REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*
18-11-2002

2. REPORT TYPE
STTR FINAL REPORT

3. DATES COVERED *(From - To)*
28JUN01-15JAN02

4. TITLE AND SUBTITLE
AUTONOMOUS DISTRIBUTED SYSTEMS - APPLICATION OF ULTRA LOW POWER TECHNOLOGY

5a. CONTRACT NUMBER
N00014-01-M-0218

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
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5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

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8. PERFORMING ORGANIZATION REPORT NUMBER
ADS-STTR-P1-FINAL

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research (ONR321)
Ballston Tower One
800 North Quincy Street
Arlington, Va 22217

10. SPONSOR/MONITOR'S ACRONYM(S)
ONR

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

20030210 065

13. SUPPLEMENTARY NOTES

14. ABSTRACT
Report Developed under STTR contract for topic N01-T001.

The primary goal of this STTR was the identification of specific components within the Deployable Autonomous Distributed System electronics that would benefit most from Ultra-Low-Power technology by examining their requirements and application environments. Specifically, the selection of a processor device was targeted.
The application of Ultra-Low-Power electronics to the Processor Module of the current DADS can save significant power, especially in the Digital Signal Processing, and widescale application in the 2010 implementation of the DADS can save even more power, using SoC technology to increase functionality and reduce area.
Advances in our ULP technology will keep us well ahead of the state-of-the-art up through the 2010 implementation.

15. SUBJECT TERMS
STTR Report, Ultra Low Power, Microelectronics, VLSI, CMOS, DADS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Brian Smith
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL	15	19b. TELEPHONE NUMBER *(include area code)* 410-990-1890

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Background

Technical Abstract:

The problem:

Deployable Autonomous Distributed Sensors are required to operate for long periods of time on a fixed energy storage quantity. The processing required of the sensor data requires high-speed digital electronics. These two are not often compatible. Commercial electronics are being used in the current implementation of the DADS electronics, the prototypes favoring operational features over power reduction. Commercial industry trends in semiconductor power consumption is toward a gradual reduction, but not quickly enough to meet the needs of advanced Navy systems. There are indications that most commercial devices will prioritize increased performance over reduced power consumption, this despite the trend to portable, handheld devices in the commercial markets. Our Ultra-Low-Power (ULP) technology is a breakthrough technology that enables devices fabricated on slightly modified standard CMOS (Complementary Metal Oxide Silicon) foundries to operate close to normal CMOS speeds (~200MHz at 0.35um) while consuming greatly reduced amounts of power.

Project Goal:

The goal of this SBIR is to advance the development of ultra low power (ULP) CMOS technology in order to produce prototype components for use in advanced networked autonomous distributed systems of sensors and other systems where minimum power consumption with high performance is the critical requirement. Power must be kept as low as possible to extend system life and reduce battery requirements, and the cost of batteries,

while at the same time providing high performance digital functionality. The development and availability of this potentially enabling technology would benefit both military and civilian applications across the board where reduced power consumption is important. This proposal builds on work that has been performed at the University of New Mexico and PicoDyne, funded by DOD and NASA, through which PicoDyne is currently developing a Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA).

Specifically, our goal is to study the feasibility of implementing a processor device in ULP for the DADS program. ASICs will also be addressed, following recommendations of DADS Navy and contractor Engineers on which device best suits the program.

Overview of Accomplishments:

On these and other DoD and internal funds, PicoDyne has developed the libraries and design flow necessary to build parts for ULP Military and Space applications. We can now start with Intellectual Property in the form of HDL (Verilog or VHDL), netlists in other technologies, or with a specification, and deliver parts meeting the required functionality, but at much reduced power consumption levels.

Technology Background

Ultra Low Power Electronics Technology

The energy consumed in a CMOS switch is the sum of the AC switching energy, DC leakage energy and short circuit energy. For the purposes of this description, the last of these will be ignored, since it represents only about 10% of the total energy and scales with voltage.

Minimum energy occurs in a CMOS circuit when DC power dissipated is equal to AC power dissipated. Consequently, maximum energy efficiency permits large off state transistor leakage currents when circuit switching activity is high, as is found in special processors (encoders, compressors, etc), digital signal processors and active general purpose processors.

The ULP approach to high performance low power circuits is to electrically adjust the threshold voltage near zero volts in active circuits, in order to optimize energy and performance according to the level of activity. This adjustment of threshold voltage is controlled by the substrate bias. The threshold voltage on the transistors is set so that the drain current when the transistor is on, divided by the drain current when the transistor is off, is approximately the ratio of the logical depth divided by the circuit activity.

It is possible to achieve excellent performance at very low supply voltages, provided that the threshold voltage is also aggressively reduced. Operating at such a low voltage supply requires some form of threshold compensation to reduce process and environment induced on and off current variations; hence the need for back-bias to improve worst-case performance and manage standby power dissipation.

Noise propagation is also not thought to be a significant issue with ULP. Internal noise sources scale at least as fast as the supply voltage. Capacitive coupled noise scales as voltage, resistively coupled noise as V^2, and the inductively couple noise as V in the short-channel limit and as V^3 in the long-channel limit. Thermal noise does not scale but is only about 100 μV. Relative noise margins tend to degrade with aggressively scaled thresholds but are still large enough to support a broad range of logic styles.

Measured Power Reductions

Supported by the DoD-led CULPRiT program, tests have been conducted to directly measure the performance of ULP devices against functionally equivalent devices in standard technology. Both NASA GSFC and the Johns Hopkins University Applied Physics Laboratory (APL) have flown a NASA standard Reed Solomon encoder. This is a 1.2um, gate array implementation, designed by the microelectronics Research Center at the University of New Mexico and operated at 12 MHz. This same design was re-implemented on the AMI .35um process at 3.3 volts, and on the AMI ULP process at 0.5 volts.

These devices were then tested at 12 MHz using the same data set for all three designs. As shown in figure 1, the power reduction over the existing flight part was a factor of 333, while the savings by the ULP part over the conventional 3.3um part was a factor of 120. These results were achieved with the first production run of ULP technology and are considered conservative. Similar reductions in power consumption have been measured for other parts developed, including the C50 DSP and the 8051 microcontroller.

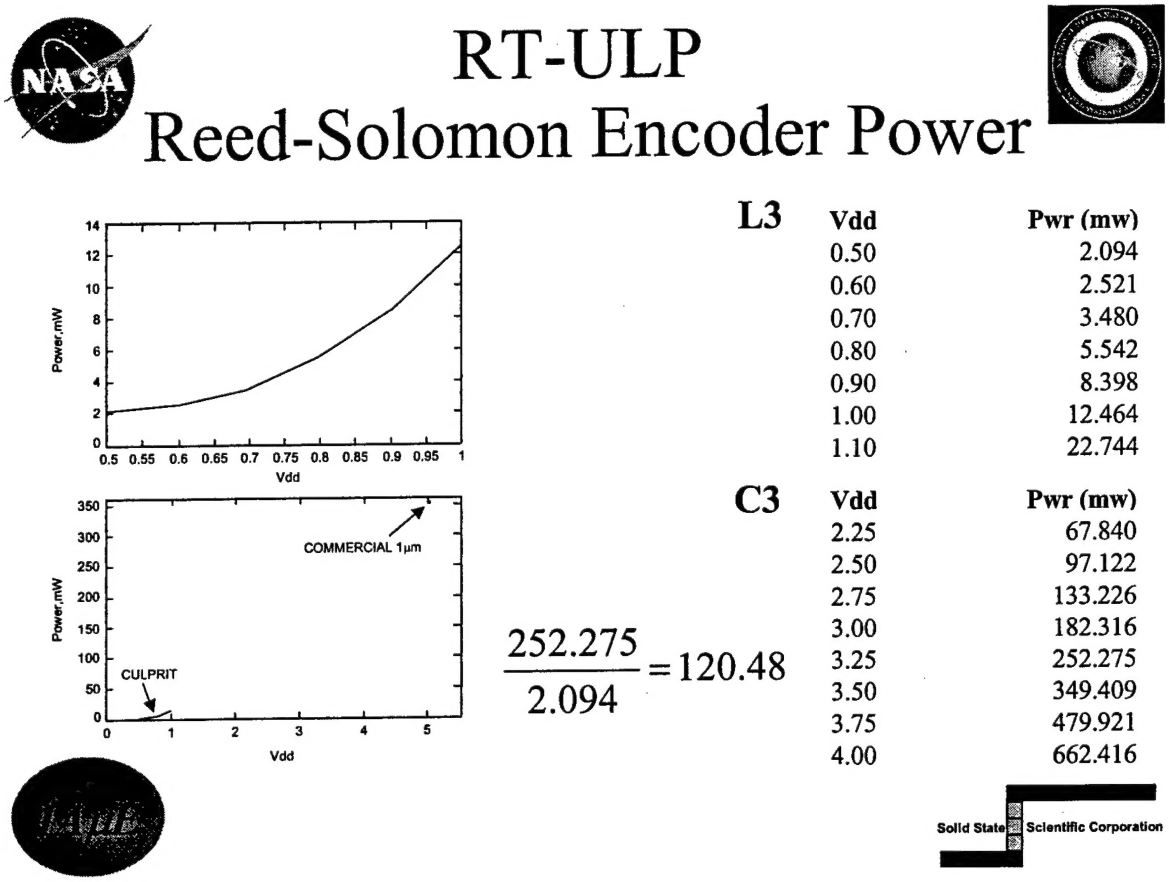

Figure 1 – Comparison of 0.35um Commercial(C3) to ULP (L3) Power

ULP Technology Maturity

The first ULP devices were demonstrated in 1991. Since that time a great deal of modeling, simulation and building of test devices has taken place. The first ULP fabrication line has fully implemented and tested and has successfully run a significant number of devices through that line on multiple occasions. Devices are mechanically similar to standard CMOS devices and have functioned as expected. While the target supply voltage for ULP technology demonstration is currently set at a conservative 0.5 Volts. Devices have been demonstrated to operate at a supply voltage below 100 mVolts.

Several chips have been fabricated and tested, including the Reed Solomon encoder described above. These devices have been operated at frequencies up to 29 MHz to this point, but it is anticipated that operation at 75 MHz will not be a serious challenge. The C50 DSP that was fabricated in early 2002 met speed requirements at greatly reduced power levels with respect to the commercial part.

Work Performed

Discussions were held with technical representatives of SPAWAR San Diego (DADS exploratory sensor node developers) first to gather documentation on the performance requirements of the current and future DADS implementations.

Review of the "Deployable Autonomous Distributed System Undersea Surveillance Node Air Deployment, Packaging and Power Consumption Study" by Mr. Tom Roy of SPAWARSYSCEN and Mr. Bill King of USSI, dtd 9 March 2000 gave us many of the current values and future goals for the system electronics. Currently, the exploratory development system is estimated to use 40 to 50 Watts of continuous average power. The unit is powered by a non-renewable energy storage system, so once deployed, the operational life is a function of the power consumption and the amount of energy available in the system. The goals of the program are to extend the current life of the node significantly. This will require advances in the sensors and communication electronics used, as well as process advances such as ours, to enable great reductions in power requirements for the processing and control electronics. Current projections are to reduce power in the sensor-node package

by an order of magnitude by 2010. Using ULP, we have demonstrated Two-Orders-Of-Magnitude power savings over implementations in current state-of-the-art electronics. Given the methods of implementation for ULP processes and circuits, we can apply these techniques to newer processes as they are developed to reduce power even more.

The paper points out that greater power reductions in electronics will be achieved by using System-on-Chip (SoC) implementations over Field Programmable Gate Array or piece-part implementations. PicoDyne has been targeting its research at exactly that market. We have been developing libraries and methodologies to allow us to gather Intellectual Property (IP) cores for processors, protocol devices, random custom logic, interface logic, and memory, and implement them onto a monolithic ULP device.

A primary goal for this project was to evaluate the feasibility of implementing a processor device in ULP. We researched available IP, resulting in the following candidate architectures at the top of the list for implementation in Phase II:

√ SUN PicoJAVA processor core
Available as RTL IP from Sun Microsystems
IP Cost – free for research, negotiate for licensing later
PicoDyne has the RTL in-house on research license from SUN Microsystems. Not well supported, but support likely to grow, especially since it executes JAVA code directly.

√ PowerPC603 general-purpose processor
32-bit – IP available from Mentor Graphics
IP Cost $500k
Available in HDL form, may be built on any CMOS process. No dynamic logic included in design (good).

√ MIPS R4k general-purpose embedded processor
32-bit – IP available from IPS
IP Cost under $500k
Available in HDL form, may be built on any CMOS process. No dynamic logic included in design (good). Many implementations exist.

Of the above processors, the MIPS R4k is the best candidate as either a stand-alone processor, or as the central core in an SoC. The bus architecture is simple and well-defined, and several SoC architectures are supported either through MIPS IP or through third parties. This allows the inclusion of other standard IP cores for the various functions required. Such IP could consist of signal conditioning for sensors, communications, housekeeping, data compression, and security encoding and decoding. This approach will allow compression of logic from several chips on a board into one SoC. Since much of the power expended on electronics boards is for inter-chip communication, including several devices on one chip greatly reduces power.

We held meeting with MIPS engineers to discuss the viability of our design approach to build devices based on their IP. We determined that we have the design base in place to perform this task. Using our in-house ULP libraries, design flow, and simulation capability, we can receive, modify as appropriate, and synthesize the R4k design into a ULP netlist, perform layout, and build a part using the ULP foundry.

In discussing alternatives with engineers from USSI, we also determined that it would be beneficial to gather custom logic into one ULP device to save power also. Once further design is completed on the prototype version of the Undersea Sensor Node, partitioning

could be performed to determine which portion of the design should be built in ULP in parallel with the off-the-shelf implementation for comparison. In the short term, it was recommended that a high-performance general purpose processor or DSP be implemented.

PicoDyne also has expertise in building logic immune from the effects of high-energy particles, which tend to cause upsets to commercial logic. As feature sizes decrease, this occurs even in terrestrial and undersea environments. We feel that the addition of our Radiation Tolerant design techniques to the ULP we have developed will be essential for system reliability in the 2005 timeframe and beyond.

Summary

During the course of this STTR, we determined that the DADS Undersea Sensor Node would gain functionality and extend on-station life through the use of ULP in the sensor electronics. Also, we determined that we can apply ULP to both the general purpose and DSP processor functions, and to general logic, combining them to create an SoC that would even further reduce power required.

Work Remaining

For Phase II, we recommend the development of a ULP MIPS R4k embedded processor, along with peripheral functions to be determined during the first part of the project by working with SPAWARSYSCEN and USSI engineers. Also, given the long-term development schedule of the DADS program, we recommend that the ULP process be applied to a smaller geometry part then the 0.35um we currently use. We foresee reducing

operating voltages down to 0.25V from 0.5V when that move is made, providing an additional 4x in power savings.